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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,297	11/07/2001	Dongyun Lee	594728112US	1257

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EXAMINER	
VITAL, PIERRE M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,297	LEE ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-22 and 24-36* is/are rejected.

7)☒ Claim(s) *4 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed December 21, 2004 in response to PTO Office Action mailed July 23, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, no claims have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-36 are now pending in this application.

3. The objection to the drawings has been withdrawn due to the amendment filed December 21, 2004.

4. The objection to the disclosure has been withdrawn due to the amendment filed December 21, 2004.

Response to Arguments

5. Applicant's arguments filed December 21, 2004 have been fully considered but they are not persuasive. As to the remarks, applicant asserted that Sonnier does not "use a plesiosynchronous technique" as recited in the claims.

Examiner respectfully traverses applicant's argument for the following reasons. As described in the specification in Paragraph 0010, "a plesiosynchronous clocking technique can be used to avoid the need to transmit a separate clock signal or derive the clock signal from the data signal. With plesiosynchronous clocking (also known as

"plesiochronous" clocking), the transmitting and receiving devices have clocks with nominally the same clock frequency". Examiner would like to point out that Sonnier discloses the use of clock with the same frequency as detailed in col. 68, lines 62-65. The clock signal that Sonnier transmits with the data is not separate from the data since Sonnier discloses that the clock signal accompanies the symbol stream (i.e., data) as detailed in col. 68, lines 47-50. By having a clock signal that accompanies the data, it is clearly seen that Sonnier provides a stream with an inherent clock signal (also defined as plesiochronous). See Davidson et al. US Pat. 6,826,199, col. 1, lines 28-30 (newly cited reference introduced to support this definition). Thus, it can be clearly seen that Sonnier discloses the use of "a plesiosynchronous technique".

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 5-7, 8, 10-21 and 24-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Sonnier et al (US5,574,849).

As per claim 1, Sonnier discloses a memory device comprising: a memory [*memory 28*; Fig. 2]; and a plurality of ports for accessing the memory of the memory device [*ports 0-5 of router 14 and X and Y ports of CPU 12*; Figs. 1A, 1B], each port having a

serial communications link for receiving from and transmitting to an accessing device [*TNet links LA connecting routers 14A and 14B*; Fig. 1B], each port using plesiosynchronous technique to receive symbols and using in-band symbols to transmit data [*command/data symbols to be transmitted out of X and Y encoders*; col. 27, lines 30-38; *T_clock and Rcv clock are of the same frequency*; col. 68, lines 62-65; *the clock signal accompanies the symbol stream*; col. 68, lines 47-50]; and out-of-band symbols to transmit control information [*Y encoder transmits IDLE symbols or other symbols used to perform control functions*; col. 28, lines 31-35].

As per claim 19, Sonnier discloses a memory device comprising: a memory that reads and writes data [*memory 28*; Fig. 2]; a multiphase clock generator that provides a multiphase clock signal [*clock generator 654*; Figs. 24 and 25; *phase comparator 660 detects a phase difference*; col. 67, lines 17-29]; and a plurality of ports [*ports 0-5 of router 14 and X and Y ports of CPU 12*; Figs. 1A, 1B], each port for connecting to a serial communications link and for receiving data and control information via the serial communications link using a plesiosynchronous technique [*command/data symbols to be transmitted out of X and Y encoders*; col. 27, lines 30-38; *Y encoder transmits IDLE symbols or other symbols used to perform control functions*; col. 28, lines 31-35; *T_clock and Rcv clock are of the same frequency*; col. 68, lines 62-65], wherein each port uses the generated multiphase clock signal generated by the multiphase clock generator [*clock oscillator 652 is used for developing the M_clock signal for both CPUs 12*; col. 67, lines 40-59].

As per claim 20, Sonnier discloses data is sent using in-band symbols [*command/data symbols to be transmitted out of X and Y encoders*; col. 27, lines 30-38]; and control information is sent via out-of-band symbols [*Y encoder transmits IDLE symbols or other symbols used to perform control functions*; col. 28, lines 31-35].

As per claims 2 and 21, Sonnier discloses each serial communications link is connected to an accessing device via a point-to-point connection [*TNet links LA connecting routers 14A and 14B are directly connected from one port to the other*; Fig. 1B].

As per claims 5 and 24, Sonnier discloses the memory includes multiple banks and wherein multiple banks can be simultaneously accessed by different ports [*Mcs 26a and 26b run in parallel to provide a path between the memory array and the interfaces 24a, 24b; and one Mc is connected to simultaneously access consecutive even addresses*; Fig. 2; col. 46, lines 7-22].

As per claims 6 and 25, Sonnier discloses each bank includes multiple sections and wherein multiple sections can be simultaneously accessed by different ports [*one Mc is connected to simultaneously access consecutive even addresses; the other Mc is similarly connected to access odd addresses*; Fig. 16; col. 46, lines 23-35].

As per claims 7 and 26, Sonnier discloses multiple sections and wherein multiple sections can be simultaneously accessed by different ports [*one Mc is connected to simultaneously access consecutive even addresses; the other Mc is similarly connected to access odd addresses*; Fig. 16; col. 46, lines 23-35].

As per claims 8 and 27, Sonnier discloses the multiple sections are configurable on a port-by-port basis [*establishing redundant communication paths between any CPUs 12, router 14A', in port 4, out port 3*; col. 13, lines 19-34].

As per claim 28, Sonnier discloses the memory device of claim 27 including the configuration information storage [*ports 4 and 5 may vary from the other ports 0-3 of the router 14*; col. 6-11].

As per claims 10 and 29, Sonnier discloses the ports are connected to the memory using time-division multiplexing [*incoming symbols are buffered and passed to MUX 104*; col. 22, lines 22-30; *each symbol is clocked out and passed to the storage and processing units by MUX 104*; col. 25, lines 2-13].

As per claims 11 and 30, Sonnier discloses the ports are connected to the memory using a crossbar switch [*the routers provide a cross-link path from one end to the other*; Fig. 1A; col. 12, lines 12-28].

As per claims 12 and 31, Sonnier discloses control information is transmitted as a primitive [*X and Y encoders transmit IDLE symbols or other symbols to perform control functions*; col. 28, lines 31-35].

As per claims 13 and 32, Sonnier discloses a primitive includes two out-of-band symbols [*both X and Y encoders transmit IDLE symbols or other symbols to perform control functions*; col. 28, lines 31-35].

As per claims 14 and 33, Sonnier discloses control information includes a synchronization symbol [*SYNC command symbol*; col. 26, lines 18-35].

As per claims 15 and 34, Sonnier discloses the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device [*a constant stream of symbols is always being transmitted from all ports*; col. 24, lines 8-61].

As per claim 16, Sonnier discloses the ports share a single multiphase clock generator [*clock generator 654*; Fig. 24; col. 67, lines 1-13].

As per claims 17 and 35, Sonnier discloses the multiphase clock generator is a phase lock loop [*all clock signals are phase-locked to M_Clk*; col. 67, lines 12-14].

As per claims 18 and 36, Sonnier discloses a synchronization symbol encodes a memory command [*command symbols communicates between various CPUs and I/O packets interfaces. Simplifying design, the processor will construct a data structure in memory*; col. 16, lines 39-53].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonnier et al (US5,574,849) and Jeong et al (US6,229,859).

As per claims 3 and 22, Sonnier discloses the claimed invention as detailed above in the previous paragraphs. However, Sonnier does not specifically teach oversampling data as recited in the claims.

Jeong discloses oversampling data for the purpose of synchronizing the operation of the receiver's clock signal with that of the transmitter (col. 3, lines 49-56).

However, oversampling data is well known in the art for generating an oversampled data stream for the purpose of synchronizing the operation of the receiver's clock signal with that of the transmitter as evidenced by Jeong.

Since the technology for oversampling data was well known and since oversampling data synchronizes the operation of the receiver's clock signal with that of the transmitter, an artisan would have recognized the advantage of oversampling data as taught by Jeong in the system of Sonnier. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply Jeong's teaching of oversampling data because it was well known to synchronize the operation of the receiver's clock signal with that of the transmitter as taught by Jeong.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sonnier et al (US5,574,849) and Lee (US5,276,642).

As per claim 9, Sonnier discloses the claimed invention as detailed above in the previous paragraphs. However, Sonnier does not specifically teach configuration information enabling certain sections of the bank as recited in the claim.

Lee discloses configuration information enabling certain sections of a bank is well known in the art for the purpose of allowing a split read/write operation of parallel read and write sections (col. 8, lines 30-38).

However, configuration information enabling certain sections of a bank is well known in the art for the purpose of allowing a split read/write operation of parallel read and write sections as evidenced by Lee.

Since the technology for implementing configuration information enabling certain sections of a bank was well known and since configuration information enabling certain sections of the bank allows a split read/write operation of parallel read and write sections, an artisan would have recognized the advantage of implementing configuration information enabling certain sections of the bank as taught by Lee in the system of Sonnier. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply Lee's teaching of configuration information enabling certain sections of the bank because it was well known to allow a split read/write operation of parallel read and write sections as taught by Lee.

Allowable Subject Matter

11. Claims 4 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not teach or suggest "each port includes a line driver with a fixed driver portion and a variable driver portion for DC-balancing" in combination with the other elements set forth in the claimed invention.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach memory accessing through a plurality of ports; using in-band symbols to transmit data and out-of-band symbols to transmit control information.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 18, 2005

Pierre M. Vital
Examiner
Art Unit 2188